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SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/086, 976	07/02/93	BULUCEA	C M7992DUS
		BSM1/1229	CARROLLE EXAMINER
		EDWARD C. KWOK 25 METRO DRIVE SUITE 700 SAN JOSE, CA 95110	ART UNIT PAPER NUMBER <i>12</i> 2508
			DATE MAILED: <i>12/29/94</i>

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

This application has been examined Responsive to communication filed on *05/26/94* This action is made final.

A shortened statutory period for response to this action is set to expire 03 month(s), 0 days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. Notice of References Cited by Examiner, PTO-892.
2. Notice of Draftsman's Patent Drawing Review, PTO-948.
3. Notice of Art Cited by Applicant, PTO-1449.
4. Notice of Informal Patent Application, PTO-152.
5. Information on How to Effect Drawing Changes, PTO-1474..
6. _____

Part II SUMMARY OF ACTION

1. Claims *17 26 29* are pending in the application.
Of the above, claims _____ are withdrawn from consideration.
2. Claims _____ have been cancelled.
3. Claims _____ are allowed.
4. Claims *17 26 29* are rejected.
5. Claims _____ are objected to.
6. Claims _____ are subject to restriction or election requirement.
7. This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. Formal drawings are required in response to this Office action.
9. The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are acceptable; not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. The proposed additional or substitute sheet(s) of drawings, filed on _____, has (have) been approved by the examiner; disapproved by the examiner (see explanation).
11. The proposed drawing correction, filed _____, has been approved; disapproved (see explanation).
12. Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has been received not been received been filed in parent application, serial no. _____; filed on _____.
13. Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. Other

EXAMINER'S ACTION

*PTO-328 (Rev. 2/93)
EPC/94*

We have entered as Paper No. 11 the AMENDMENT filed 03 October 1994. We however are unable to discern any proposed amendment in Paper No. 11 but, rather, REMARKS essentially in traverse of the rejections applied in Paper No. 8. Notwithstanding the Applicants' characterization of Paper No. 11 as an amendment, we instead regard Paper No. 11 as a request for reconsideration.

On page 2 the Applicants, in the same vein, choose to hold that our characterization of Tonnel as showing a trench DMOS transistor is incorrect. The Applicants characterize the Tonnel device instead as a VMOS transistor.

In response, we believe that both characterizations are consistent with the Tonnel transistor. The Applicants' VMOS terminology indicates a substantial Vertical current path in the Metal Oxide Semiconductor (VMOS) transistor; and our trench DMOS terminology indicates that Tonnel formed insulated gate electrode (32) within a trench etched into semiconductor substrate material (21) whereby the transistor was constructed in a vertical Diffused manner. Hence the "D" component of the DMOS acronym. Tonnel chose to characterize as slots (30) whereas we chose to synonymously characterize slots (30) instead as trenches to emphasize our point of view that the Tonnel trench DMOS transistor falls well within the scope of Applicants' Claim 17. We presently find that our characterization of the Tonnel transistor is entirely consistent with DMOS terminology as used by Blanchard '535, Reference AA presently provided by the Applicants. We thus conclude therefrom that the Applicants' traverse of our characterization of the Tonnel transistor as a trench DMOS transistor has little and insufficient merit - especially in view of the fact that VMOS terminology constitutes a mere distinction without any difference whatsoever.

Further in the request for reconsideration the Applicants indicate that Tonnel provides no explicit teaching within the "detailed description" regarding the depth relationships shown in the cross-sectional views of Figures 12 and 19 of complete embodiments. The Applicants dismiss each and every cross-sectional view of Figures 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18 and 19 as being "merely fortuitous" because they "contradict" the perspective view of Figure 3. The Applicants conclude therefrom that Tonnel does not appreciate the depth relationships claimed and, thereby does not enable one to make the Invention claimed.

In response, we respectfully disagree on all counts. We more particularly find no detailed description - just a description fully adequate to meet the requirements of 35 U.S.C. 101 and 35 U.S.C. 112. We don't expect Applicants to provide detailed descriptions sufficient for one to take without modification or embellishment to a semiconductor foundry for providing commercial product. We further don't expect Applicants to provide detailed descriptions of prior art information that one of ordinary skill would have brought to a reading of Tonnel. In another example, Tonnel provides no information whatsoever about optimization of packing density with desirable channel length and width parameters, certainly important considerations for obtaining a successful commercial product. As a measure of ordinary skill at the time of Tonnel, we look to the Lisiak et al. article, presently provided as a reference of interest. We expect one of ordinary skill at the time of Tonnel to have possessed ordinary skill and to have brought the Lisiak et al. information to a reading of Tonnel. One would have optimized the Tonnel products with respect to device parameters not at all discussed by Tonnel,

but in accordance with the Lisiak et al. prior art information. Among the many parameters discussed by Lisiak et al. we find the optimized nonplanar MOS transistors like that of Tonnel should have channel lengths of at least one micron, with Lisiak et al. teaching 1.5 microns in particular. Such is wholly consistent with slot depths of about 2 to 2.5 microns in Tonnel. As opposed to the perspective view of Figure 3 providing more top surface information than is provided with the not-to-scale, cross-sectional views of Figures 12 and 19, we would expect little and less distortion in the spatial relationships among the various elements. Tonnel clearly and unambiguously suggests that the V-shaped slots (30) be less deep than the deepest P-type sections (22) and more deep than the less deep P-type sections (25). There are no device or process parameters that can be more enhanced by making the V-shaped slots excessively deep, but deep enough to adequately penetrate the PN-junction demarking base from drain regions as in Lisiak et al. The about two micron depth of the V-shaped slots/trenches in Tonnel are not inconsistent with field oxide (23) thickness of about one micron as disclosed by Tonnel. Making the V-shaped slots (30) less deep than the less deep P-type base regions (25) would be counter to common knowledge and common sense as amply demonstrated by the Lisiak et al. embodiments of nonplanar MOS transistor structures shown with Figures 1, 2, 5, 7(a), 7(c) and 7(d). We still further find the plausible process of manufacture disclosed by Tonnel with Figures 4 to 12 as supporting our conclusion that one would have possessed sufficient common knowledge and common sense to have applied the optimized results of Lisiak et al. Tonnel first introduced P-type regions (22), shown in Figure 4, that become deeper, as shown in Figure 5, due to the thermal oxidation step to grow a micron thickness of field oxide (23). Tonnel then forms slots

(30) to about the same depth as deeper P-type regions (22), as shown in Figure 6, assuming a slot depth of about 2 to 2.5 microns after Lisiak et al. Subsequent thermal processing, e.g., forming less deep P-type regions (25) at the Figure 9 process step, causes diffusion also to take place in the deeper P-type (22) regions to advance them still deeper than slots (30). We thus experience excessive difficulty when we attempt to reconcile the clear and unambiguous method disclosed by Tonnel with the Applicants' opinion that Tonnel does not enable one to make the Invention claimed. Rather than accidentally and unintentionally showing a nonplanar MOS transistor structure that Tonnel had no expectation to envisage or to make, as essentially advanced by the Applicants, we conclude from the preponderance of evidence that one of ordinary skill at the time of Tonnel would have understood Tonnel as clearly, unambiguously and deliberately disclosing at least a structure fully consistent with the Invention claimed and a method of making the structure.

On page 3 of the request for reconsideration the Applicants advance the same reasons, as discussed *supra*, to support their belief that pending Claims 17 and 29 are not obvious over Patent Claim 2.

In response, we believe that the reasons advanced by the Applicants are insufficient to meet the double patenting rejections. We find that Patent Claim 2 claims everything defined by pending Claim 17. In a "one-way" determination, all that is needed here, it is well settled that omission of elements defined in Patent Claim 2 would have been an obvious expedient, i.e., omission of the elements whose function is not needed would have been obvious to one of ordinary skill. In a "two-way" determin-

ation we rely upon Tonnel to show obviousness of obvious elements within Patent Claim 2, e.g., the "heavily doped" characterization of the substrate material. We thus conclude that the basis for the Applicants' belief is insufficient.

Not discerning a reasonable basis to conclude the Invention claimed is patentable, we maintain Claim rejections as expressed in Paper No. 8, incorporated herein by reference thereto.

We again reject all Claims.

THIS ACTION IS MADE FINAL.

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IF A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 CFR 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

An inquiry concerning this communication may be directed to Examiner J. Carroll at telephone number 703-308-4926, or to the Group 2500 Receptionist at telephone number 703-308-0956.

Respectfully Submitted,

JAMES J. CARROLL
EXAMINER
ART UNIT 253